

ABSTRACT OF THE DISCLOSURE

Disclosed is a semiconductor memory device which shortens an external access time when there is contention
5 between an external access and an internal access. The semiconductor memory device includes an arbiter which receives a first entry signal for entering a first access mode (external access) and a second entry signal for entering a second access mode (internal access) and
10 determines priority of the first and second access modes in accordance with an order of receipt of the first and second entry signals. The arbiter sequentially generates a first mode trigger signal corresponding to the first entry signal and a second mode trigger signal corresponding to the
15 second entry signal in accordance with the determined priority. The arbiter executes the first access mode by priority over the second access mode when the arbiter is supplied with the first entry signal with a predetermined period after the second access mode has been determined to
20 have priority.